Laboratory 4

(Due date: June 11th)

OBJECTIVES

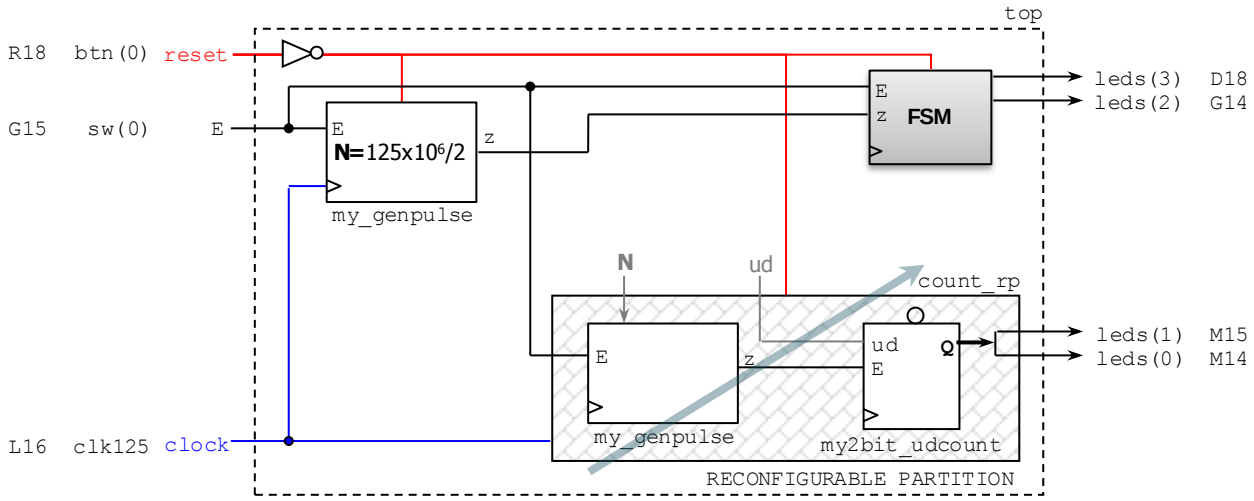
- ✓ Learn the Partial Reconfiguration (PR) flow using the Vivado TCL console.
- ✓ Generate: i) full bitstreams, ii) partial bitstreams, and iii) blanking bitstreams.
- ✓ Perform partial reconfiguration on the ZYBO (or ZYBO Z7-10) Board using the JTAG interface.

REFERENCE MATERIAL

- ✓ Refer to the Tutorial: Embedded System Design for Zynq PSoC for information on the Partial Reconfiguration Flow using the Vivado TCL console as well as examples.

FIRST ACTIVITY (100/100)

- Download the project files (my_dynled.zip) of the LED Pattern Control example (1 RP) available in the Unit 6 of the Tutorial: Embedded System Design for Zynq PSoC.
  - ✓ `top_io.xdc`: File associated with the ZYBO Board. The I/O pinout shown in the figure corresponds to ZYBO Board pins. If using the ZYBO Z7-10 Board, you must create your own `top_io.xdc`.
- This circuit contains only 1 Reconfigurable Partition (RP), with 2 parameters (`N`, `ud`).
- I/O signals:
  - ✓ `reset`: Active-high reset connected to `BTN0` in the ZYBO (or ZYBO Z7-10) board
  - ✓ `E` (enable): This input is connected to `SW0` in the ZYBO (or ZYBO Z7-10) Board.
  - ✓ `clock`: This is an external clock to the Zynq PL running at 125 MHz.
  - ✓ `leds[3..0]`: Connected to `LED3-LED0` in the ZYBO (or ZYBO Z7-10) Board.



- Follow the procedure detailed in the Tutorial, but generate 4 configurations (you will need to edit the `design.tcl` file):
  - ✓ `count_rp`: Up counter, count changing every 1 second.
  - ✓ `count_rp`: Up counter, count changing every 0.5 seconds
  - ✓ `count_rp`: Down counter, count changing every 1 second.
  - ✓ `count_rp`: Down counter, count changing every 0.5 seconds.

- Generate the 4 partial bitstreams, the 4 full bitstreams, along with the blanking bitstream.
- Partial Reconfiguration demo: Download the corresponding hardware bitstreams on the Zynq PSoC to demonstrate that each of the four configurations (and the blanking configuration) work when loading the partial bitstreams. **Demonstrate this to your instructor**.

- Submit (as a .zip file) the following to Moodle (an assignment will be created). DO NOT submit the whole PR project.
  - ✓ The /Sources folder: This contains all the sources (.vhd, .xdc) files.
  - ✓ The /Bitstreams folder: This contains all the bitstreams.
  - ✓ The design.tcl file.

Instructor signature: _____ **Date:** _____